# ELIOTT OODS

Volume 1: FUNCTIONAL SPECIFICATION Part 3: OPTIONAL UNITS

Section 1: MULTIPLEXER

## Contents

					]	Page
Chapter	1:	INTRODUCTION			• • •	1
					÷.,	
Chapter	2:	MULTIPLEXER INSTRUCTIONS				
		2,1 Group Selection				2
		2.2 Optional Channel Grouping	• . • •			3
		2.3 Expander		Ξ.		3
Chapter	3:	INTERRUPT, RESET and POWER ON			¥.	
		3.1 INTERRUPT				4
		3.2 RESET				
		3.3 POWER ON				
Chapter	4:	GENERAL				
Â		4.1 Power Supplies		• .•		5
		4.2 Environmental Conditions				5
		4.3 Physical Dimensions				5

# Chapter I: INTRODUCTION

The 903 Multiplexer facilitates the use of more than one 903 peripheral device with the 903 central processor. It makes available up to eight sets of peripheral sockets (hereafter called channels).

The eight channels are divided into two groups, all channels within a group being parallel connected. The groups, which are referred to as groups A and B, are selected by the appropriate multiplexer instruction (see paragraph 2.1). Once a group is selected each peripheral attached to that group receives all subsequent peripheral instructions. When a group is deselected no peripheral instructions can affect the peripherals attached to that group:

As it is normally required that only one peripheral shall respond to a particular instruction, each of the 903 peripherals is assigned a number within the range 0 to 15, which is defined by bits 8 to 11 of the instruction code address. This number is known as the peripheral class number. Thus only a peripheral of the specified class number will respond to instructions given to the group of parallel channels.

Peripherals of the same class number should be connected to different groups.

Bits 12 and 13 of the instruction address are not transmitted to the peripherals: they are decoded by the central processor and specify a shift, or paper tape station instruction, or a peripheral input or output instruction. The central processor sets the logical interface signals for input or output data transfer when a peripheral input or output instruction is detected. These signals control all transfers to and from the peripherals. Bits 1-11 are transmitted to all peripherals along the address lines.

An N. P. L. Interface Matching Unit may be connected direct to the central processor peripheral socket or one of the Multiplexer channels making available the increasingly wide range of peripherals conforming to this standard. (see Section 1. 3. 2).

# 903 1.3.1.

# Chapter 2: MULTIPLEXER INSTRUCTIONS

A group of 903 instructions are reserved for addressing the Multiplexer which is assigned a class number 15. (It is assigned a peripheral class number for addressing purposes only, it is not a peripheral).

2. Group Selection

Group selection uses address bits 1 and 2 and these have the following effects:

Instruc	ction		Effect
Function	Address	the second se	
15	6016	bit $1 = 0$ ) bit $2 = 0$ )	Multiplexer address: groups A and B are not selected. Should any peripheral instruction, other than class 15, be given now the 903 central processor will be held up.
15	6017	bit 1 = 1 ) bit 2 = 0 )	Select group A deselect group B: subsequent peripheral instructions will be diverted to group A channels only.
15	6018	bit 1 = 0 ) bit 2 = 1 )	Select group B deselect group A; subsequent peripheral instructions will be diverted to group B channels only.
15	6019	bit 1 = 1 ) bit 2 = 1 )	Select both groups A and B: subsequent peripheral instructions will be passed to all channels on groups A and B.

2 (Issue 2) 903 1.3.1.

## Chapter 2: MULTIPLEXER INSTRUCTIONS

A group of 903 instructions are reserved for addressing the Multiplexer which is assigned a class number 15. (It is assigned a peripheral class number for addressing purposes only, it is not a peripheral).

A modification is available as an option to allow ARCH system peripheral devices to be controlled through the Multiplexer. Its effect is to prevent instructions with class 15 address code from being transmitted through the Multiplexer. This enables ARCH equipment to be used, and in no way affects the operation of any peripherals designed for the 903.

## 2.1 Group Selection

Group selection uses address bits 1 and 2 and these have the following effects:

Instruction			
Function	Address		Effect
15	6016	bit 1 = 0 ) bit 2 = 0 )	Multiplexer address: groups A and B are not selected. Should any peripheral instruction, other than class 15, be given now the 903 central processor will be held up.
15	6017	bit 1 = 1 ) bit 2 = 0 )	Select group A deselect group B: subsequent peripheral instructions will be diverted to group A channels only.
15	6018	bit 1 = 0 ) bit 2 = 1 )	Select group B deselect group A: subsequent peripheral instructions will be diverted to group B channels only.
15	6019	bit 1 = 1 ) bit 2 = 1 )	Select both groups A and B: subsequent peripheral instructions will be passed to all channels on groups A and B.

3<sup>.</sup> (Issue 2)

# 2.2 Optional Channel Grouping

groupings:

Multiplexers are available with the following channel

		`A		$\mathbf{B}$
		0	and	2
	or	2	and	2
	or	4	and	2
• .	or	6	and	2

or with all sockets wired in parallel for use as a simple Expander (see below).

2.3 Expander

When used as a simple Expander all signals from the peripheral interface pass to all peripherals and there is no group selection; thus, peripherals with overlapping instruction codes may not be used together on an Expander. 903 1.3.1.

## Chapter 3: INTERRUPT, RESET and POWER ON

# 3.1 INTERRUPT

The three level interrupt system is independent of prevailing group or channel selection conditions. The central processor receives interrupts at all three levels as though from a single peripheral device, all peripheral interrupts of the same level being transmitted along the same line.

#### 3.2 RESET

RESET is transmitted to all peripherals irrespective of group selection. When RESET occurs both groups A and B are selected by the Multiplexer logic.

# 3.3 POWER ON

The POWER ON signal line is not available at the Multiplexer channel sockets.

Chapter 4: GENERAL

## 4.1 Power Supplies

D.C. power supply requirements may usually be met by existing power supply capacity. Typical figures are:

Туре	+6 V D.C.	-6 V D.C.
2 channel	1.4A	56 mA
4 channel	2.15A	82 mA
6 channel	3.1A	126 mA
8 channel	3,85A	152 m.A

If this is not available a separate peripheral power supply unit will be required.

4.2 Environmental Conditions

The Multiplexer will operate over the full range of 903 computer operating conditions which are:

Temperature 10<sup>o</sup> to 30<sup>o</sup>C

Relative Humidity 20% to 95% (without condensation)

4.3 Physical Dimensions

The Multiplexer, whether 2, 4, 6 or 8 channels, occupies three  $8\frac{3}{4}$  in. x 19 in. internal racks in a 903 cabinet.